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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/067,599	04/28/98	ALLISON S	RA998-007

TM02/0228

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EXAMINER	
CHANNAVAJJALA,S	
ART UNIT	**PAPER NUMBER**
2177	16

DATE MAILED: 02/28/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/067,599	ALLISON ET AL.	
	Examiner	Art Unit	
	Srirama Channavajjala	2177	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/5/2001 [CPA]* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Response to CPA

1. The request filed on February 05, 2001 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on Application No. 09/067,599 is acceptable and a CPA has been established, paper no. # 8.

   An action on the CPA follows.

2. Examiner acknowledges applicant's Preliminary Amendment, paper no. # 9, filed on February 05, 2001.

3. Claims 15-34 are remain pending in this application.

4. Claims 1-14 have been canceled, paper no. # 9.

5. Examiner acknowledges receipt of Applicant's Amendment filed on August 10, 2000, paper no. # 5.

6. Claims 1, 8-9, 12-14 have been amended, paper no. # 5.

Drawings

7. The Drawing filed on 4/28/98 are not objected to by the Draftsperson under 37CFR 1.84 or 1.152, [see PTO-948, paper no.# 3].

Information Disclosure Statement

8. The information disclosure statement filed on 4/28/1998, paper no. # 2 has been considered and a copy was enclosed. [see paper no. # 3].

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

9. Claims 15-16, 19-20, 33 and 36 are rejected under 35 U.S.C. 102(e) as being anticipated by Dosiere et al., [hereafter Dosiere], US Patent No. 577800.

10. As to Claims 15,19, and 33, Dosiere details a system which including 'a first memory in which a set of patterns are stored' [col 2, line 4-5, col 4, line 47-48, col 5, line 20-22, col 10, line 22-23], examiner notes that Dosiere uses first m-bit set are in the first memory, fig 3a represents part of the first memory, see col 7, line 38-39 , 'a second memory' [col 2, line 7-9, col 5, line 20-22], Dosiere specifically details first memory and second memory, containing m-bit set forms n-bit pattern bits, 'identifying patterns in the first memory to be matched against the data' [col 1, line 62-67, col 4, line 56-64], Dosiere's teachings including bit-by-bit comparison, examiner interpreting matching data to be equivalent to Dosiere's including bit-by-bit comparison, 'mask data' [col 2, line 46-60]; 'pattern match logic circuit arrangement correlating marked patterns in said first memory against the data ' [col 5, line 20-37].

11. As to Claims 16 and 20, Dosiere details a system which including 'marked patterns are fewer than the total number of patterns in said first memory' [col 4, line 54-61].

12. As to Claim 36, Dosiere details a system which including 'pointers include mask bits' [col 6, line 27-29, line 49-52, see fig 2a-2b, 3a-3b].

13. Claims 33-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Williams et al., [hereafter Williams], US Patent No. 5938771.

14. As to Claims 33-34, Williams details a system which including 'pattern matching or providing a set of patterns' [fig 2, element 60, col 4, line 50-53], examiner interpreting pattern matching or providing a set of patterns are to be equivalent to Williams fig 2, element 60 because it associated with Pattern Match signal from the pattern match logic, element 60, see col 4, line 56-57; 'network to wake station connected to the communications network' [see col 3, line 27-35, see fig 1], 'network interface cared' [fig 1B, element 10], 'providing data to be matched with selected patterns' [col 4, line 56-62], 'providing pointers for identifying the selected patterns' [col 5, line 31-42, line 43-50], examiner interpreting pointers are inherent aspect of Williams because firstly Williams teachings including read/write operations depended on the bit status from the register 76a, secondly, Magic Packet logic element 62 has the ability to scan incoming frames with specific addresses as detailed in col 5, line 43-45, thirdly, pointer(s) is a variable that simply contains the memory location or memory address of some data

rather than the data itself, and address is specifying a location in the memory where data is stored is well known in the art; 'correlating the data with the selected patterns' [col 6, line 4-13], 'generating a match signal if the data and the selected patterns match' [col 6, line 25-44]

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

15. Claims 17- 18, 21-32 rejected under 35 U.S.C. 103(a) as being unpatentable over Dosiere et al., [hereafter Dosiere], US Patent No. 5778000 as applied to claim15, 19 above, and further in view of Jeng, US Patent No. 5892768.

16. As too Claim 21, Dosiere details a system which including 'a first memory in which a set of patterns are stored' [col 2, line 4-5, col 4, line 47-48, col 5, line 20-22, col 10, line 22-23], examiner notes that Dosiere uses first m-bit set are in the first memory, fig 3a represents part of the first memory, see col 7, line 38-39 , 'a second memory' [col 2, line 7-9, col 5, line 20-22], Dosiere specifically details first memory and second memory, containing m-bit set forms n-bit pattern bits, 'identifying patterns in the first memory to be matched against the data' [col 1, line 62-67, col 4, line 56-64], Dosiere's teachings including bit-by-bit comparison, examiner interpreting matching data to be equivalent to Dosiere's including bit-by-bit comparison, 'mask data' [col 2, line 46-60]; 'pattern match logic circuit arrangement correlating marked patterns in said first memory against the data ' [col 5, line 20-37]. Dosiere does not specifically detail 'network interface circuit'. Jeng details a system which including 'network interface circuit' [fig 2, col 1, line 13-17, col 3, line 55-67].

It would have been obvious one of the ordinary skill in the art at the time of the applicant invention to combine the concepts taught by Jeng with the system of Dosiere because receiving data from a network allows access to much more information than access in local memory of Dosiere [see Dosiere, col 7, line 38-39 a second memory col 2, line 7-9, col 5, line 20-22] and thus improving the communication of computer data in a network more specifically store and forward [col 1, line 45-49].

17. As to Claims 17 and 22 Dosiere does not specifically teach 'data is received from a network', although Dosiere teaches data manipulation between first and second memory [see col 5, line 21-23]. Jeng details a system which including 'data is received from a network' [col 2, line 13-17, col 2, line 41-44], more specifically, Jeng teaches Ethernet media independent interface, see fig 2.

It would have been obvious one of the ordinary skill in the art at the time of the applicant invention to combine the concepts taught by Jeng with the system of Dosiere because receiving data from a network allows access to much more information than access in local memory of Dosiere [see Dosiere, col 7, line 38-39 a second memory col 2, line 7-9, col 5, line 20-22] and thus improving the communication of computer data in a network more specifically store and forward [col 1, line 45-49].

18. As to Claim 18 and 29, Jeng teaches a system which including 'first state machine for assembling data received from a network into predetermined sizes' [col 2, line 41-46], examiner interpreting predetermined sizes to be equivalent to Jeng's 4-bit data packets converted into 8-bit data packets [see fig 5B]; Dosiere teaches ' identifying beginnings and endings of data frames' [col 5, line 56-59], 'a second state machine operatively coupled to the first state machine' [col 1, line 45-47], 'second state machine including circuit that receives the predetermined sizes from the first state machine' [col 2, line 11-25], although generating addresses for accessing the first and second memory are inherent aspect of Jeng's teachings because Jeng specifically teaches for example buffer memory, see fig 2, elements 50, and 52, more specifically,

Dosiere teaches addresses for accessing data, see fig 3a, col 7, line 38-47; 'pattern and mask data are to be read and used with the predetermined sizes in generating the first control signal' [see fig 4, col 8, line 39-67, col 9, line 1-7]

19. As to Claim 23, Jeng details for example local area network or LANs , WANs using Ethernet network [see col 1, line 6-9], therefore, examiner notes that host computer coupled to the system interface is inherent aspect of Jeng's teaching; although Jeng teaches for example frames having data packets essentially comprising multiple bit packets [see col 2, line 44-59], more specifically, Dosiere teaches patterns and mask data [see fig 1, col 2, line 61-67, col 3, line 1-27, col 4, line 26-29].

20. As to Claim 24, Jeng teaches 'network interface' [fig 2], Jeng teaches for example destination address and source address [see col 1, line 50-67], also Jeng teaches for example each packet of data associated with signal bit [see col 2, line 51-57], therefore, Jeng teaches the limitation of claim 24.

21. As to Claim 26, Jeng details 'patterns are arranged contiguously in the pattern storage' [see fig 2, elements 50 and 52].

22. As to Claim 27-28, Dosiere teaches patterns and mask data [see fig 1, col 2, line 61-67, col 3, line 1-27, col 4, line 26-29], specifically, m-bit set forms part of n-bit pattern [see col 2, line 55-50, col 5, line 43-48, line 65-67], Jeng teaches 'network interface' [fig 2].

23. As to Claims 31-32, Jeng details a system which including 'PCI interface' and 'Ethernet MII interface' [fig 2-3, fig 7, col 6, line 13-27].

24. As to Claim 25, Jeng does not teach 'each pattern in the set of patterns are arranged in 4 byte wide words and 128 byte sectors', however, Jeng suggested using for example 4 byte cyclical redundancy code or CRC and 64-1500 byte data field [see col 1, line 53-56]

It would have been obvious of the ordinary skill in the art at the time of applicant invention to arranging various different byte size words and byte sectors because it not only provides flexibility, but also, saves memory space, thus improving the responsiveness of the system.

25. As to Claim 30, Jeng does not detail 'address generation circuit uses the expression YYYxxxxx to determine the addresses for the pattern RAM, wherein xxxxx represents an index count and YYY represents states for a state machine.', although Jeng suggested for example using a 10-Base Ethernet system for transmitting data packets from source addresses to the destination address [see col 1, line 17-19]

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to assign one bit or multiple bits 'Y' for state machine, multiple bits 'x' for index count because predetermined address of one bit or multiple bits saves memory space, improving the pattern matching and responsiveness of the system.

Response to Arguments

26. Applicant's arguments in the paper no. # 9, filed on February 05, 2001 with respect to new Claims 15-36 have been considered but are moot in view of the new ground(s) of rejection.

27. Also, Examiner acknowledges "Declarations traversing grounds of rejection under 37 CFR 1.132" along with the Preliminary Amendment filed with a Continued Prosecution application, paper no. # 9.

Conclusion

The prior art made of record

a.	US Patent No.	5778000
b.	US Patent No.	5892768
c.	US Patent No.	5938771

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Srirama Channavajjala whose telephone number is (703)308-8538. The examiner can normally be reached on Monday-Friday from 7:00 AM to 3:30 PM Eastern time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Breene, can be reached on (703)305-9790. The fax phone number for this Art Unit is (703)308-6606.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703)305-9600.

cs

February 23, 2001.

John E. Breene

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